

IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): An image processor comprising:

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a control unit configured to control the transfer of image data to predetermined destinations;

AV
a switch configured to divide the image data into m x n pixels based on a first command from the control unit, the image data having n lines with m pixels per one line, and the switch further configured to transfer each one of the n lines of the image data to [[a]] one of the predetermined destination destinations based on a second command from the control unit;

a storage unit including (n-1) number of memories each configured to store one line of the n lines of the image data;

a control unit configured to control the transfer of the each one of the n lines of the image data to the predetermined destination;

a compression unit configured to batch compress the image data of m x n pixels based on a third command from the control unit,

wherein said control unit is further configured to:

control said switch to directly transfer (n-1) lines of the n lines of the image data to a first destination of the predetermined destinations, the first destination being the (n-1) number of memories, and

directly transfer a remaining one line of the n lines of the image data directly to a second destination of the predetermined destinations, the second destination being said compression unit; and

[[to]] control the storage unit to transfer the (n-1) lines of the image data stored in the (n-1) number of memories to said compression unit, and